What is claimed is:

1. A capacitor of a semiconductor device, the capacitor comprising:

a capacitor lower electrode on a semiconductor substrate;

a dielectric layer on the lower electrode, remote from the semiconductor substrate; and

an upper electrode on the dielectric layer,

wherein the upper electrode comprises a metallic layer on the dielectric layer, remote from the lower electrode, and an $Si_{1-x}Ge_x$ layer on the metallic layer, remote from the dielectric layer.

2. The capacitor of Claim 1, wherein the lower electrode comprises a doped polysilicon layer.

3. The capacitor of Claim 2, wherein the dielectric layer comprises an $HfO_2$ layer, an $Al_2O_3$ layer and/or an $Al_2O_3/HfO_2$ composite layer.

4. The capacitor of Claim 1, wherein the lower electrode comprises a metallic layer.

5. The capacitor of Claim 4, wherein the dielectric layer comprises an $HfO_2$ layer, an $Al_2O_3$ layer, an $Al_2O_3/HfO_2$ composite layer, an $HfO_2/Al_2O_3$ layer, a $SrTiO_3$ layer, and/or a (Ba, Sr) $TiO_3$ layer.

6. The capacitor of Claim 1, wherein the $Si_{1-x}Ge_x$ layer comprises a doped poly$Si_{1-x}Ge_x$ layer.

7. The capacitor of Claim 6, wherein the doped poly$Si_{1-x}Ge_x$ layer is doped with P or As.

8. The capacitor of Claim 6, wherein the doped poly$Si_{1-x}Ge_x$ layer is doped with B.

9. The capacitor of Claim 8, wherein a doping concentration of B is more than or equal to $1x10^{20}/cm^3$.

10. The capacitor of Claim 1, wherein x satisfies $0.05 \leq x \leq 0.9$.

11. The capacitor of Claim 1, wherein the metallic layer of the upper electrode comprises TiN, WN, TaN, Cu, W, Al, noble metals, an oxide of the noble metals, and/or combinations thereof.

12. The capacitor of Claim 1 wherein the capacitor lower electrode comprises a cylinder type capacitor lower electrode.

13. A capacitor of a semiconductor device, the capacitor comprising:

a cylinder type capacitor lower electrodecomprising a metallic layer, on a semiconductor substrate;

a dielectric layer on the cylinder type lower electrode, remote from the semiconductor substrate; and

an $Si_{1-x}Ge_x$ upper electrode on the dielectric layer, remote from the cylinder type lower electrode.

14. The capacitor of Claim 13, wherein the dielectric layer comprises an $HfO_2$ layer, an $Al_2O_3$ layer, an $Al_2O_3/HfO_2$ composite layer, an $HfO_2/Al_2O_3$ layer, a $SrTiO_3$ layer, and/or a (Ba, Sr) $TiO_3$ layer.

15. The capacitor of Claim 13, wherein the metallic layer comprises TiN, WN, TaN, Cu, W, Al, noble metals, oxide of the noble metals, and/or combinations thereof.

16. The capacitor of Claim 13 wherein the $Si_{1-x}Ge_x$ upper electrode comprises a doped poly$Si_{1-x}Ge_x$ upper electrode.

17. A method of fabricating a capacitor of a semiconductor device, the method comprising:

forming a capacitor lower electrode on a semiconductor substrate;

forming a dielectric layer on the lower electrode; and

sequentially stacking a metallic layer and an $Si_{1-x}Ge_x$ layer on the dielectric layer to form an upper electrode comprising the metallic layer and the $Si_{1-x}Ge_x$ layer.

18. The method of Claim 17 wherein the $Si_{1-x}Ge_x$ layer comprises a doped poly$Si_{1-x}Ge_x$ layer.

19. The method of Claim 18, wherein the doped poly$Si_{1-x}Ge_x$ layer is formed by doping a poly$Si_{1-x}Ge_x$ layer with P or As.

20. The method of Claim 18, wherein the doped poly$Si_{1-x}Ge_x$ layer is formed by doping a poly$Si_{1-x}Ge_x$ layer with B.

21. The method of Claim 18, wherein the doped poly$Si_{1-x}Ge_x$ layer is formed by depositing a poly$Si_{1-x}Ge_x$ layer while simultaneously doping impurities.

22. The method of Claim 18, wherein the doped poly$Si_{1-x}Ge_x$ layer is deposited and simultaneously activated.

23. The method of Claim 22, wherein the $Si_{1-x}Ge_x$ is deposited and simultaneously activated between about 350°C and about 550°C.

24. The method of Claim 18, wherein the doped poly$Si_{1-x}Ge_x$ layer is deposited and then activation and thermal treatment is performed.

25. The method of Claim 24, wherein activation and thermal treatment is performed between about 400°C and about 550°C.

26. The method of Claim 17, wherein the metallic layer of the upper

electrode comprises TiN, WN, TaN, Cu, W, Al, noble metals, oxide of the noble metals, and/or combinations thereof.

27. The method of Claim 17, wherein the doped poly$Si_{1-x}Ge_x$ layer is formed using low pressure chemical vapor deposition (LP CVD) using furnace type equipment, single wafer type equipment, and/or mini-batch equipment.

28. The method of Claim 17, wherein the lower electrode comprises a metallic layer.

29. A method of fabricating a capacitor of a semiconductor device, the method comprising:

forming a capacitor lower electrode on a semiconductor substrate;

forming a dielectric layer on the lower electrode; and

forming an $Si_{1-x}Ge_x$ layer on the dielectric layer at about 550°C or less.

30. A method according to Claim 29, further comprising:

thermally treating the $Si_{1-x}Ge_x$ layer at about 550°C or less.